74HC393; 74HCT393

Dual 4-bit binary ripple counter

Rev. 03 — 6 September 2005 Product data sheet

1. General description

The 74HC393; HCT393 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC393; 74HCT393 contains 4-bit binary ripple counters with separate clocks (1$\overline{CP}$ and 2 $\overline{CP}$) and master reset (1MR and 2MR) inputs to each counter.

The operation of each half of the 74HC393; 74HCT393 is the same as the 74HC93; 74HCT93, except no external clock connections are required.

The counters are triggered by a HIGH-to-LOW transition of the clock inputs.
The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets (1MR and 2MR) are active-HIGH asynchronous inputs to each 4-bit counter. A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

2. Features

- Two 4-bit binary counters with individual clocks
- Divide by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC393						
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V				
	n$\overline{CP}$ to nQ0		-	12	-	ns
	nQx to nQ(x+1)		-	5	-	ns
	nMR to nQx		-	11	-	ns
$f_{clk(max)}$	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	-	99	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance (per gate)	[1] [2]	-	23	-	pF

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Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HCT393						
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V				
	$n\overline{CP}$ to nQ0		-	20	-	ns
	nQx to nQ(x+1)		-	6	-	ns
	nMR to nQx		-	15	-	ns
$f_{clk(max)}$	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	-	53	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance (per gate)	[1] [3]	-	25	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] V_I = GND to V_{CC}

[3] V_I = GND to V_{CC} – 1.5 V

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC393N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC393D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC393DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC393PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HC393BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT393N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT393D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT393DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT393PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT393BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

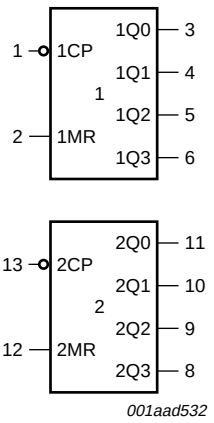


Fig 1. Logic symbol

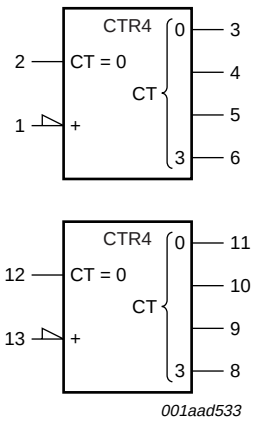


Fig 2. IEC logic symbol

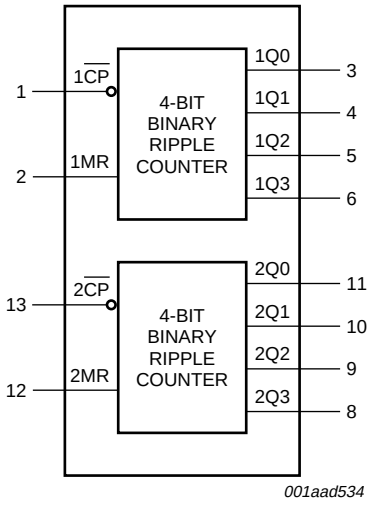


Fig 3. Functional diagram

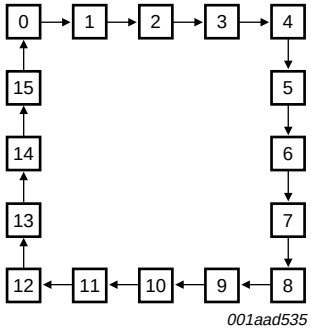


Fig 4. State diagram

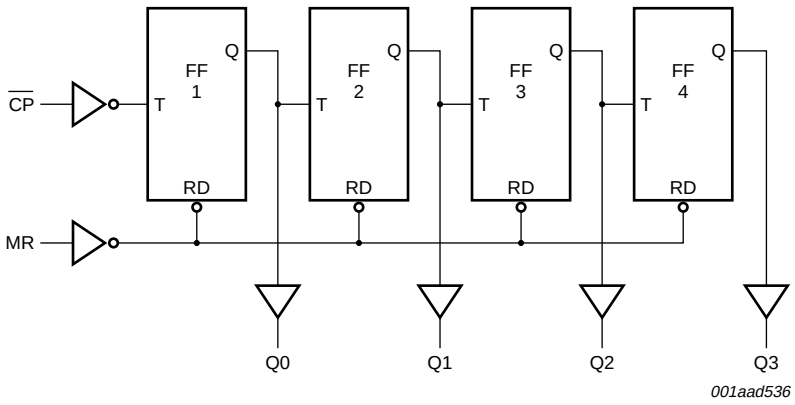


Fig 5. Logic diagram (one counter)

6. Pinning information

6.1 Pinning

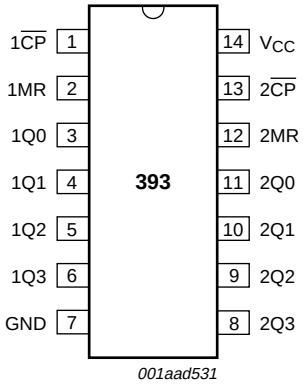
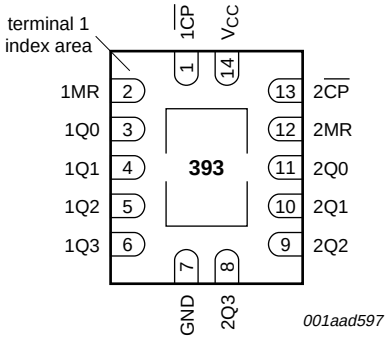


Fig 6. Pin configuration SO14; DIP14 (T)SSOP14



Transparent top view

Fig 7. Pin configuration DHVQFN14

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1$\overline{CP}$	1	1 clock input (HIGH-to-LOW, edge-triggered)
1MR	2	1 asynchronous master reset input (active HIGH)
1Q0	3	1 flip-flop output 0
1Q1	4	1 flip-flop output 1
1Q2	5	1 flip-flop output 2
1Q3	6	1 flip-flop output 3
GND	7	ground (0 V)
2Q3	8	2 flip-flop output 3

Table 3: Pin description *...continued*

Symbol	Pin	Description
2Q2	9	2 flip-flop output 2
2Q1	10	2 flip-flop output 1
2Q0	11	2 flip-flop output 0
2MR	12	2 asynchronous master reset input (active HIGH)
$2\overline{CP}$	13	2 clock input (HIGH-to-LOW, edge-triggered)
V_{CC}	14	supply voltage

7. Functional description

7.1 Function table

Table 4: Count sequence for one counter [1]

Count	Output			
	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

[1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	quiescent supply current			-	±50	mA
I_{GND}	ground current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation					
	DIP14 package		[1]	-	750	mW
	SO14 package		[2]	-	500	mW
	(T)SSOP14 package		[3]	-	500	mW
	DHVQFN14 package		[4]	-	500	mW

[1] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC393						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
74HCT393						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 4.5$ V	-	6.0	500	ns

10. Static characteristics

Table 7: Static characteristics type 74HC393

At recommended operating conditions; voltages are referenced to GND (ground = 0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = +25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = –4 mA	3.98	4.32	-	V
		V_{CC} = 6 V; I_O = –5.2 mA	5.48	5.81	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = 4 mA	-	0.15	0.26	V
		V_{CC} = 6 V; I_O = 5.2 mA	-	0.16	0.26	V
I_{LI}	input leakage current	V_{CC} = 6 V	-	-	0.1	µA
I_{CC}	quiescent supply current	V_{CC} = 6.0 V; I_O = 0 A; V_I = V_{CC} or GND	-	-	8.0	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = –4 mA	3.98	-	-	V
		V_{CC} = 6 V; I_O = –5.2 mA	5.48	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = 4 mA	-	-	0.33	V
		V_{CC} = 6 V; I_O = 5.2 mA	-	-	0.33	V
I_{LI}	input leakage current	V_{CC} = 6 V	-	-	0.1	µA
I_{CC}	quiescent supply current	V_{CC} = 6.0 V; I_O = 0 A; V_I = V_{CC} or GND		-	80	µA

Table 7: Static characteristics type 74HC393 *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 4.5 V; I_O = –4 mA	3.98	-	-	V
		V_{CC} = 6 V; I_O = –5.2 mA	5.48	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 4.5 V; I_O = 4 mA	-	-	0.33	V
		V_{CC} = 6 V; I_O = 5.2 mA	-	-	0.33	V
I_{LI}	input leakage current	V_{CC} = 6 V	-	-	0.1	µA
I_{CC}	quiescent supply current	V_{CC} = 6.0 V; I_O = 0 A; $V_I = V_{CC}$ or GND	-	-	160	µA

Table 8: Static characteristics type 74HCT393

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 µA	4.4	4.5	-	V
		I_O = –6 mA	3.98	4.32	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	0	0.1	V
		I_O = 6.0 mA	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current (per input pin)	$V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	1$\overline{CP}$, 2$\overline{CP}$		-	40	144	µA
	1MR, 2MR		-	100	360	µA
C_i	input capacitance		-	3.5	-	pF

Table 8: Static characteristics type 74HCT393 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 μA	4.4	-	-	V
		I_O = −6 mA	3.84	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 6.0 mA	-	-	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	μA
ΔI_{CC}	additional quiescent supply current (per input pin)	V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	$1\overline{CP}$, $2\overline{CP}$		-	-	180	μA
	1MR, 2MR		-	-	450	μA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 μA	4.4	-	-	V
		I_O = −6 mA	3.7	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 6.0 mA	-	-	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	μA
ΔI_{CC}	additional quiescent supply current (per input pin)	V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	$1\overline{CP}$, $2\overline{CP}$		-	-	196	μA
	1MR, 2MR		-	-	490	μA

11. Dynamic characteristics

Table 9: Dynamic characteristics type 74HC393

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = +25 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 2.0 V	-	41	125	ns
		V_{CC} = 4.5 V	-	15	25	ns
		V_{CC} = 5 V; C_L = 15 pF	-	12	-	ns
		V_{CC} = 6.0 V	-	12	21	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 2.0 V	-	14	45	ns
		V_{CC} = 4.5 V	-	5	9	ns
		V_{CC} = 5 V; C_L = 15 pF	-	5	-	ns
		V_{CC} = 6.0 V	-	4	8	ns
t_{PHL}	propagation delay					
	nMR to nQx	see Figure 9				
		V_{CC} = 2.0 V	-	39	140	ns
		V_{CC} = 4.5 V	-	14	28	ns
		V_{CC} = 5 V; C_L = 15 pF	-	11	-	ns
		V_{CC} = 6.0 V	-	11	24	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V	-	19	75	ns
		V_{CC} = 4.5 V	-	7	15	ns
		V_{CC} = 6.0 V	-	6	13	ns
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V	80	17	-	ns
		V_{CC} = 4.5 V	16	6	-	ns
		V_{CC} = 6.0 V	14	5	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 2.0 V	80	19	-	ns
		V_{CC} = 4.5 V	16	7	-	ns
		V_{CC} = 6.0 V	14	6	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9				
		V_{CC} = 2.0 V	5	3	-	ns
		V_{CC} = 4.5 V	5	1	-	ns
		V_{CC} = 6.0 V	5	1	-	ns

Table 9: Dynamic characteristics type 74HC393 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 2.0 V	6	30	-	MHz
		V_{CC} = 4.5 V	30	90	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	99	-	MHz
		V_{CC} = 6.0 V	35	107	-	MHz
C_{PD}	power dissipation capacitance (per gate)	[1] [2]	-	23	-	pF
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay					
	nCP to nQ0	see Figure 8				
		V_{CC} = 2.0 V	-	-	155	ns
		V_{CC} = 4.5 V	-	-	31	ns
		V_{CC} = 6.0 V	-	-	26	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 2.0 V	-	-	55	ns
		V_{CC} = 4.5 V	-	-	11	ns
		V_{CC} = 6.0 V	-	-	9	ns
t_{PHL}	propagation delay					
	nMR to nQx	see Figure 9				
		V_{CC} = 2.0 V	-	-	175	ns
		V_{CC} = 4.5 V	-	-	35	ns
		V_{CC} = 6.0 V	-	-	30	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V	-	-	95	ns
		V_{CC} = 4.5 V	-	-	19	ns
		V_{CC} = 6.0 V	-	-	16	ns
t_W	pulse width					
	nCP HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V	100	-	-	ns
		V_{CC} = 4.5 V	20	-	-	ns
		V_{CC} = 6.0 V	17	-	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 2.0 V	100	-	-	ns
		V_{CC} = 4.5 V	20	-	-	ns
		V_{CC} = 6.0 V	17	-	-	ns
t_{rec}	recovery time					
	nMR to nCP	see Figure 9				
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 4.5 V	5	-	-	ns
		V_{CC} = 6.0 V	5	-	-	ns

Table 9: Dynamic characteristics type 74HC393 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 2.0 V	5	30	-	MHz
		V_{CC} = 4.5 V	24	90	-	MHz
		V_{CC} = 6.0 V	28	107	-	MHz
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 2.0 V	-	-	190	ns
		V_{CC} = 4.5 V	-	-	38	ns
		V_{CC} = 6.0 V	-	-	32	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 2.0 V	-	-	70	ns
		V_{CC} = 4.5 V	-	-	14	ns
		V_{CC} = 6.0 V	-	-	12	ns
t_{PHL}	propagation delay					
	nMR to nQn	see Figure 9				
		V_{CC} = 2.0 V	-	-	210	ns
		V_{CC} = 4.5 V	-	-	42	ns
		V_{CC} = 6.0 V	-	-	36	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9				
		V_{CC} = 2.0 V	5	-	-	ns
		V_{CC} = 4.5 V	5	-	-	ns
		V_{CC} = 6.0 V	5	-	-	ns

Table 9: Dynamic characteristics type 74HC393 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 2.0 V	4	-	-	MHz
		V_{CC} = 4.5 V	20	-	-	MHz
		V_{CC} = 6.0 V	24	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] V_I = GND to V_{CC}

Table 10: Dynamic characteristics type 74HCT393

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = +25 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 4.5 V	-	15	25	ns
		V_{CC} = 5 V; C_L = 15 pF	-	20	-	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 4.5 V	-	6	10	ns
		V_{CC} = 5 V; C_L = 15 pF	-	6	-	ns
t_{PHL}	propagation delay					
	nMR to nQn	see Figure 9				
		V_{CC} = 4.5 V	-	18	32	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 4.5 V	-	7	15	ns
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 4.5 V	19	11	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 4.5 V	16	6	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9				
		V_{CC} = 4.5 V	5	0	-	ns

Table 10: Dynamic characteristics type 74HCT393 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 4.5 V	27	48	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	53	-	MHz
C_{PD}	power dissipation capacitance (per gate)	[1] [2]	-	25	-	pF
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 4.5 V	-	-	31	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 4.5 V	-	-	13	ns
t_{PHL}	propagation delay					
	nMR to nQx	see Figure 9				
		V_{CC} = 4.5 V	-	-	40	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 4.5 V	-	-	19	ns
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 4.5 V	24	-	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 4.5 V	20	-	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9	5	-	-	ns
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 4.5 V	22	-	-	MHz
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 4.5 V	-	-	38	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 4.5 V	-	-	15	ns
t_{PHL}	propagation delay					
	nMR to nQx	see Figure 9				
		V_{CC} = 4.5 V	-	-	48	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 4.5 V	-	-	22	ns

Table 10: Dynamic characteristics type 74HCT393 *…continued*

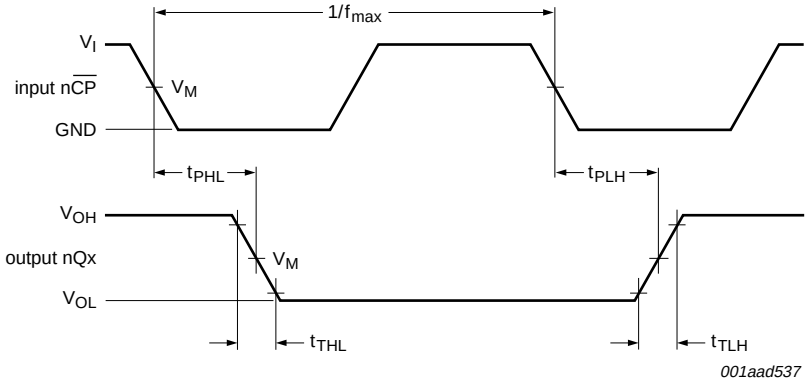
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 4.5 V	29	-	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 4.5 V	24	-	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9	5	0	-	ns
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 4.5 V	18	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

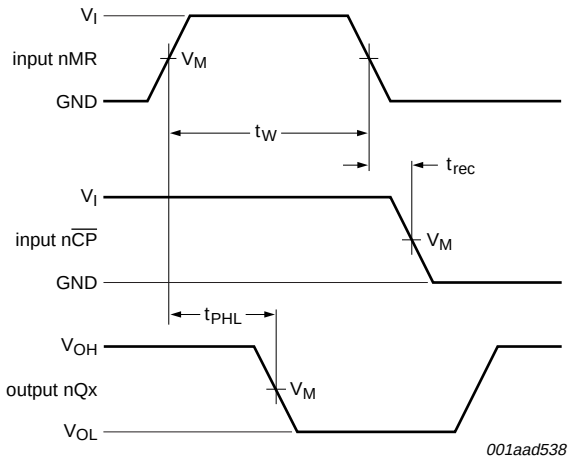
[2] V_I = GND to V_{CC} − 1.5 V.

12. Waveforms



Measurement points are given in Table 11.

Fig 8. Propagation delays clock (nCP) to output (nQx), the output transition times and the maximum clock frequency

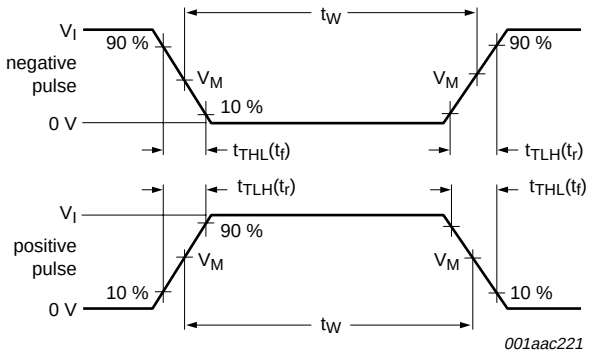


Measurement points are given in Table 11.

Fig 9. Propagation delays clock (nCP) to output (nQx), pulse width master reset (nMR), and recovery time master reset (nMR) to clock (nCP)

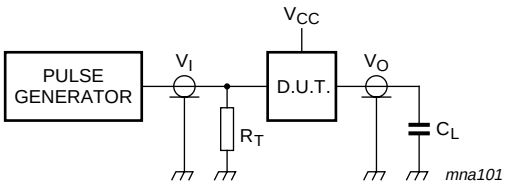
Table 11: Measurement points

Type	Input	Output
	V_M	V_M
74HC393	$0.5V_{CC}$	$0.5V_{CC}$
74HCT393	1.3 V	1.3 V



Measurement points are given in Table 11.

a. Input pulse definition



Test data is given in Table 12.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

b. Test circuit

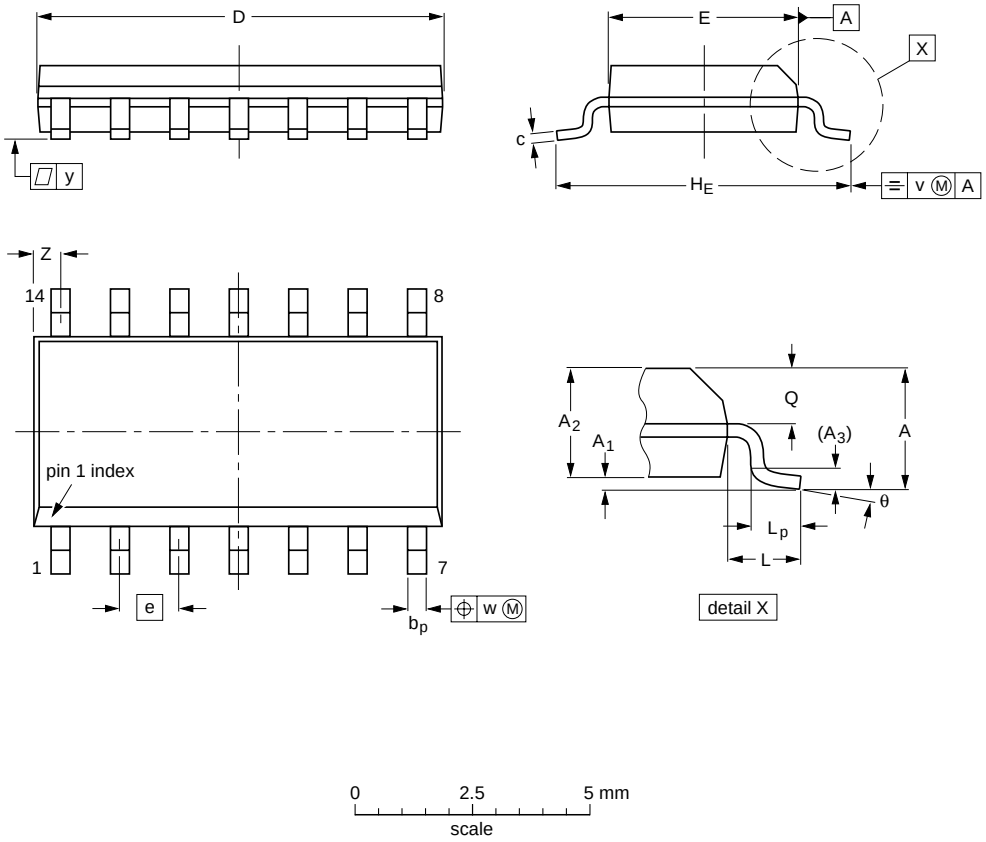
Fig 10. Load circuitry for switching times

Table 12: Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V to 6.0 V	GND to V_{CC}	6 ns	15 pF, 50 pF

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

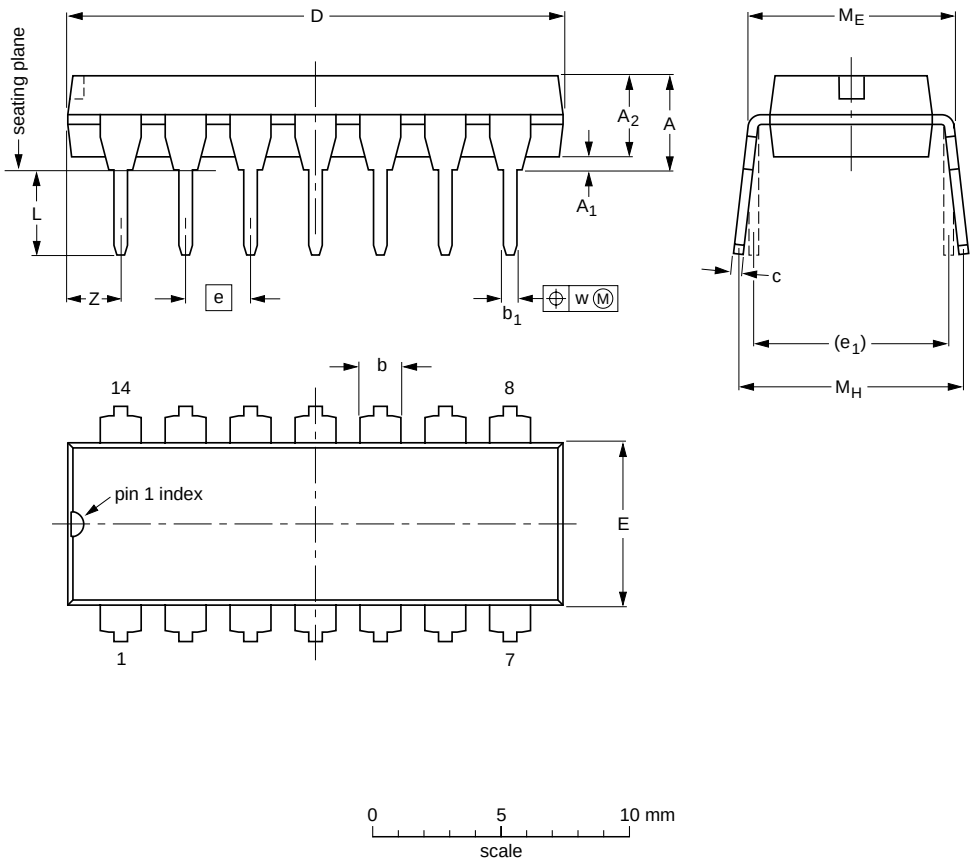
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

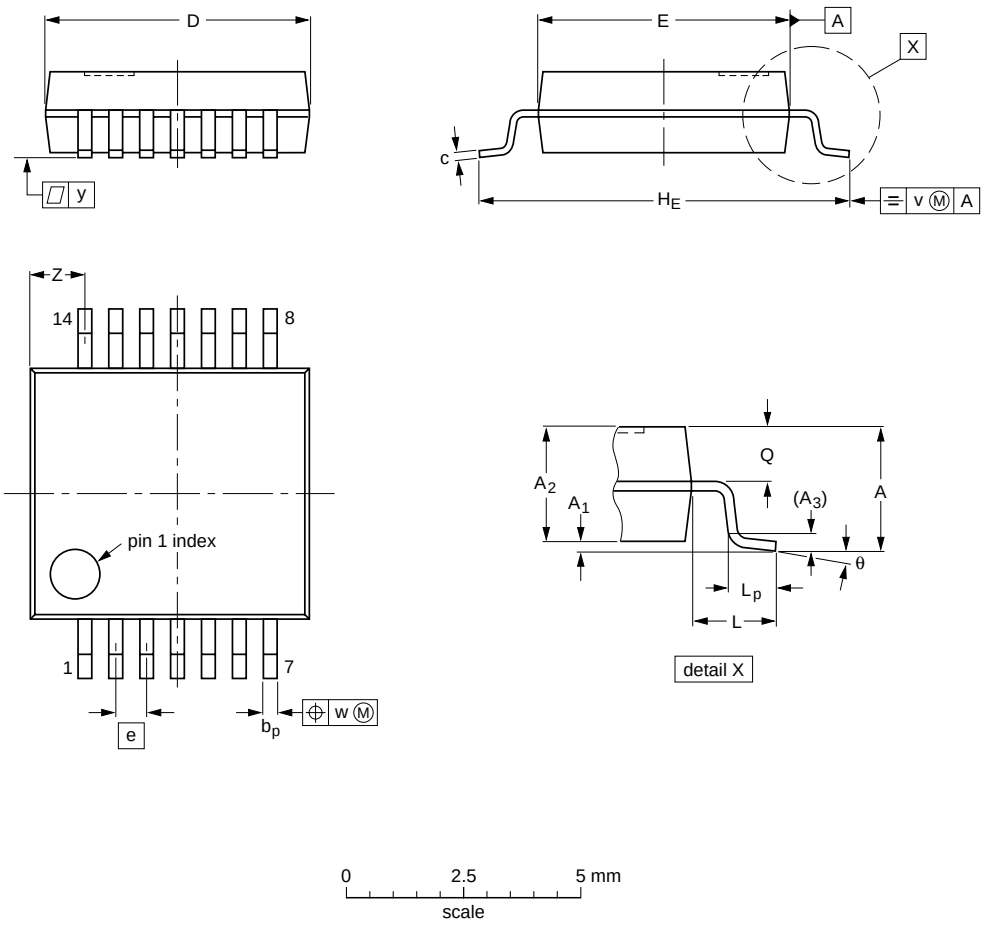
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 12. Package outline SOT27-1 (DIP14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

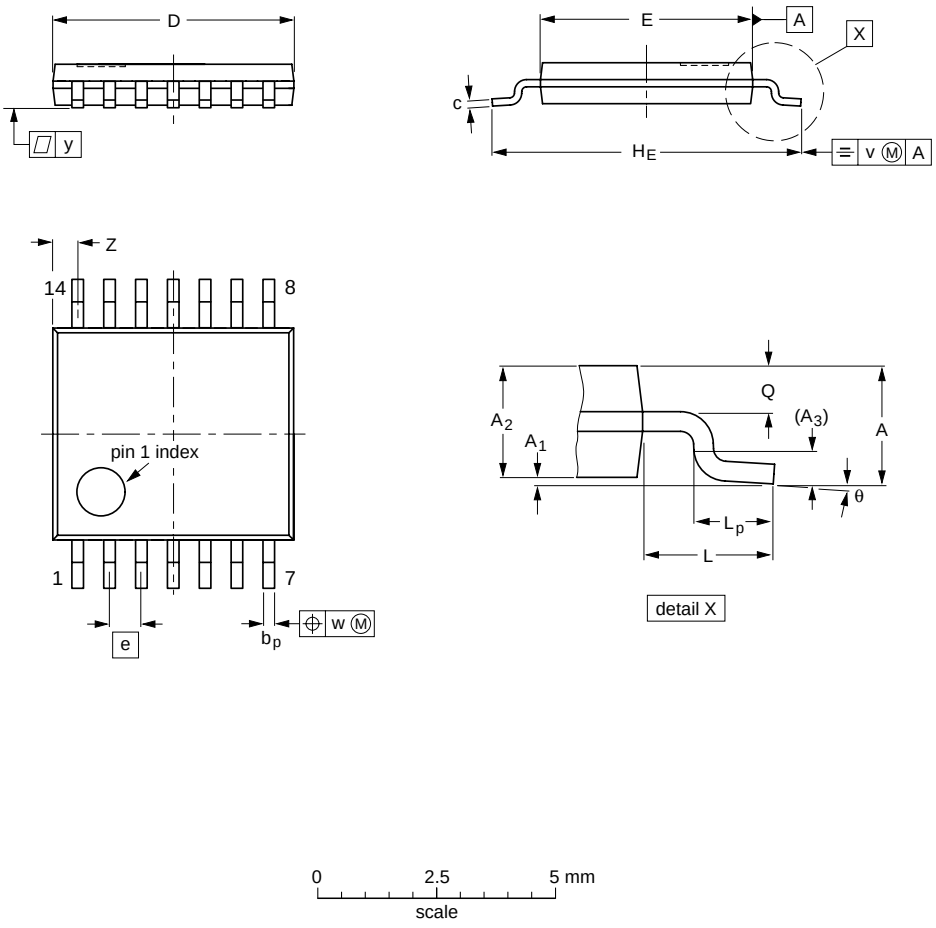
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

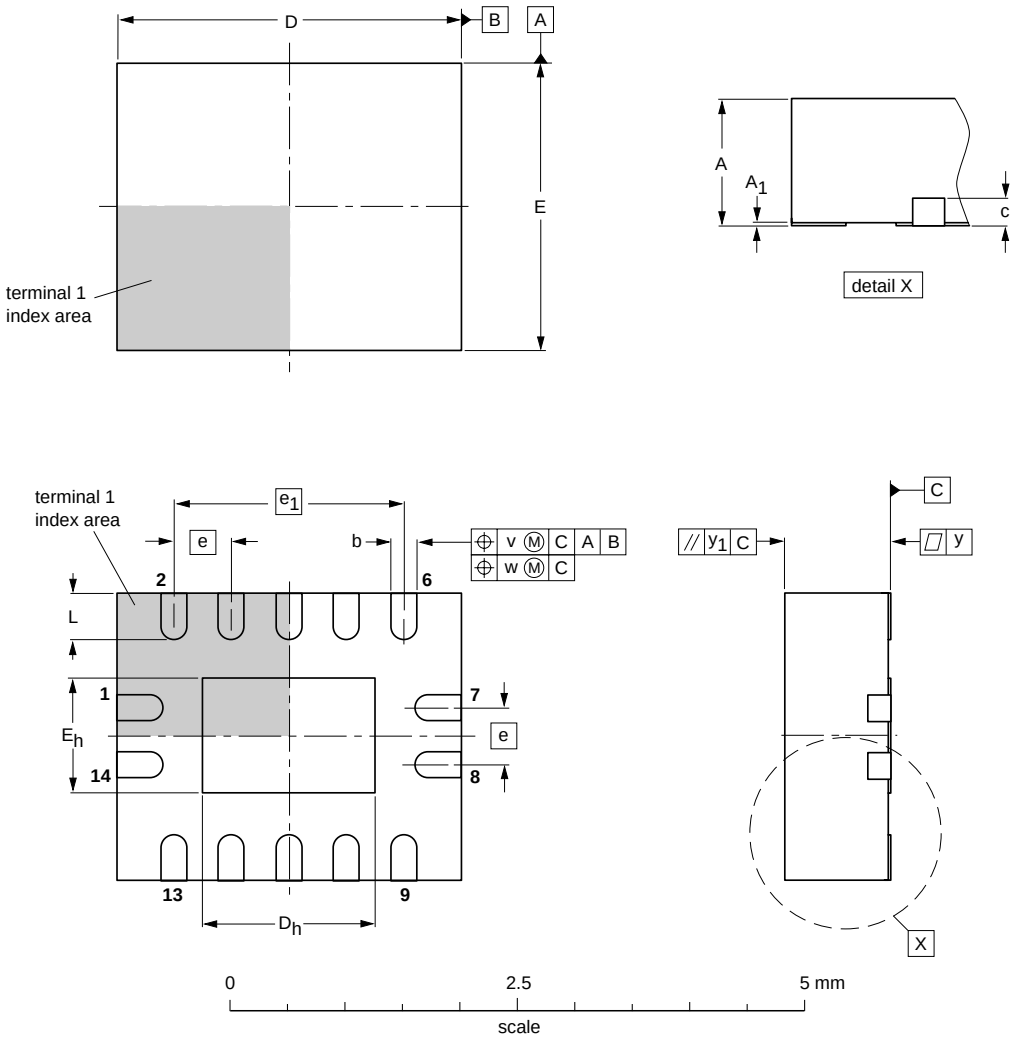
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 15. Package outline SOT762-1 (DHVQFN14)

14. Abbreviations

Table 13: Abbreviations table

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor Transistor Logic
LSTTL	Low-power Schottky Transistor Transistor Logic
DUT	Device Under Test

15. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT393_3	20050906	Product data sheet	-	-	74HC_HCT393_CNV_2
Modifications:	• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Added family specifications. • Added type numbers 74HC393BQ and 74HCT393BQ (package DHVQFN14).				
74HC_HCT393_CNV_2	19901201	Product specification			74HC_HCT393_CNV_1
74HC_HCT393_CNV_1					-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

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